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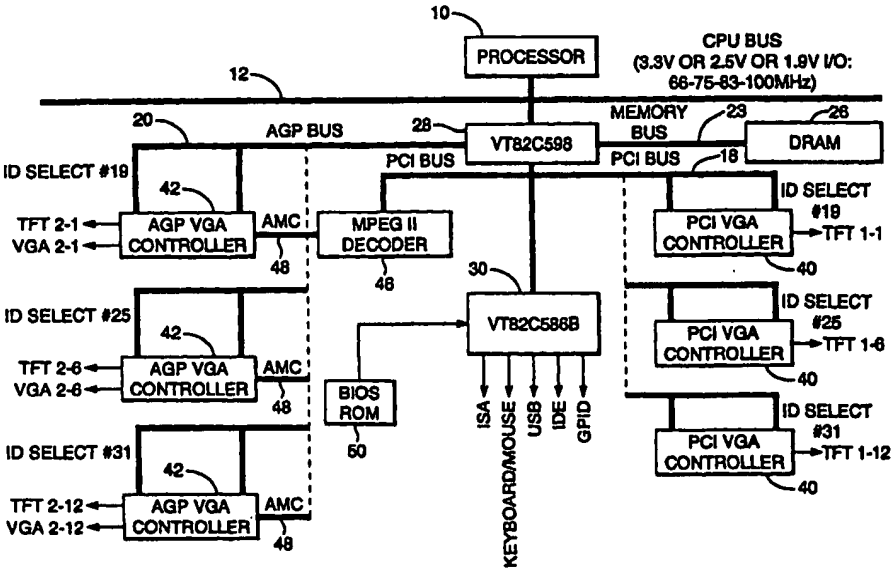

CHECKOUT CH33 EXTENDED MULTISCREEN CONFIGURATION

(57) Abstract

A standard PC architecture is modified to enable a plurality of screens to be driven from a single PC motherboard. A plurality of screen controllers is attached to the AGP bus and the bus extended correspondingly. A plurality of screen controllers is also attached to an extended PCI bus. An MPEG II decoder, on the PCI bus is attached to each of the screen controllers on the AGP bus via a multimedia channel. Each display controller is addressed by and connected to only one of the PCI and AGP buses.

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PC BASED SYSTEMS FOR DRIVING OF MULTIPLE SCREENS

This invention relates to PCs (personal computers) and is particularly concerned with the display of data to a number of screens.

Many environments exist in which it is desirable to be able to display data to a number of screens or to display different data to a number of screens from a single location. This data might include video, graphics, text etc. or a mixture of these formats.

Conventional PCs include a general purpose data bus to which a display controller is attached. Data to and from the monitor is routed on this bus. At present, a number of screens can be run from the same processor but they are limited to providing the same display. To provide a number of screens displaying potentially different data or running potentially independent applications would require a number of different processors and associated components such as system chipsets, memory etc. This is clearly expensive.

The invention aims to ameliorate this problem and to enable multiple screens to be driven from a single processor.

In its broadest form, the invention connects display controllers to more than one bus. In one preferred embodiment, a display controller is attached to a general purpose bus, such as a PCI bus and another display controller is attached to a graphics bus such as an AGP bus.

More specifically there is provided a PC computer comprising a processor, a processor bus for transfer of data to and from the processor, a graphics bus, a general purpose bus for transfer of data to and from a plurality of input and output devices, a system chipset connected to the processor, graphics and general purpose buses comprising the processor bus, the graphics bus and the

general purpose bus, a first screen controller for controlling at least one display screen connected to the general purpose bus, and a second screen controller for controlling at least one display screen connected to the graphics bus; wherein the first and second screen controllers are each addressed from only one of the general purpose and graphics buses.

Preferably, the graphics bus is an accelerated graphics port (AGP) bus.

Preferably, the general purpose bus is a peripheral component interconnect (PCI) bus.

Embodiments of the invention have the advantage that additional screen controllers can be attached to the motherboard enabling a plurality of screens to be run off the same PC processor, each potentially running on independent application.

Preferably, a video decoder is attached to the general purpose bus and to the screen controller on the graphics bus. This video decoder may be an MPEG II decoder connected over a multimedia channel which has the advantage of faster data throughput with minimum processor intervention.

Preferably, the PC controller comprises a plurality of screen controllers attached to the graphics bus.

Preferably, the PC computer comprises a plurality of screen controllers connected to the general purpose bus.

By extending the graphics bus, which may be an AGP bus, and the general purpose bus, which may be a PCI bus, a plurality of screen controllers may be connected to each bus, enabling a large number of displays to be run from a single processor unit. The number of screens is limited only by the number of device addresses that can be allocated from the system BIOS.

Preferably, said two or more screens comprise screens of different display types. By using screen controllers that can support simultaneous outputs of differential types, for example Tri-view controllers which output VGA,

TFT and TV, the number of screens which can be run from a single processor is increased still further.

The invention also provides a PC computer comprising a central processor unit (CPU) having a CPU bus associated therewith for transfer of data to and from the CPU, an accelerated graphics part (AGP) bus communicating with a graphics controller, a peripheral component interconnect (PCI) bus communicating with a plurality of peripheral components, a system chipset comprising a system controller communicating with the AGP bus, and a bridge communicating with the system controller and a plurality of further buses and devices, wherein the PCI bus communicates with the system controller and the bridge, at least one first screen controller communicating with the PCI bus, and at least one second screen controller communicating with the AGP bus, the first and second screen controllers each being addressed by one only of the PCI and AGP buses.

An embodiment of the invention will now be described, by way of example only, and with reference to the accompanying drawings in which:

Figure 1 is an overview of a conventional PC architecture;

Figure 2 is a block diagram of an architecture embodying the invention;

Figure 3 is a block diagram showing how three displays may be driven from a single board computer; and

Figure 4 shows how the PCI and AGP buses may be extended to drive a greater number of screens.

Referring to Figure 1, the architecture illustrated is a standard conventional PC architecture. A processor 10, which may for example, be a PENTIUM II (TM) processor manufactured by Intel Corporation is connected to the system or CPU bus 12. The CPU bus may operate at 66, 75, 83 or 100 MHz and at I/O voltages of 3.3V, 2.5V or 1.9V.

A second level cache memory 14 and the system chipset 16 are also connected to the CPU bus 12. A number of further buses are connected to the chipset 16, including the Peripheral Component Interconnect (PCI) bus 18; the Accelerated Graphics Port (AGP) bus 20 and the ISA (Industry Standard Architecture) bus 22. The PCI bus 18 is also manufactured by Intel Corporation and is a 32 bit bus functioning as a 64 bit bus running at 33 or 66 MHz. The PCI bus is compatible with the ISA bus and operates asynchronously. A number of expansion slots 24 are attached to the PCI bus 18. The PCI bus is one example of a general purpose bus which routes data to and from the processor and peripherals on the system.

The AGP bus relieves the PCI bus of graphics data to enable it to concentrate on duties such as transfer of data from disk drives. Thus, the AGP bus is a graphics bus which is intended to perform a dedicated function. As can be seen from Figure 2, the AGP is connected to a 3D graphics controller 25. On a conventional PC, a device on a single card can be attached to the AGP bus whereas up to 4 expansion slots can be attached to the PCI bus. The addressing for these additional devices is controlled by the system BIOS (basic input/output software) which is held in ROM and so once set cannot be changed.

The system chipset 16 functions to control the buses around the CPU, the AGP, PCI and ISA buses and, as seen from Figure 1, also controls the Dynamic RAM (DRAM) 26 via a memory bus 23. The settings of the chipset can only be changed by special BIOS software. The System Chipset also controls the second level cache memory, interfaces such as the keyboard or mouse and the Universal Serial Bus (USB). The USB bus is a serial input device which replaces connectional parts for I/O devices such as keyboard, mouse, printers etc.

One example of a suitable chipset is the VIA Apollo MVP3 chipset available from Via Corporation. This is a high performance and energy efficient chipset intended for

implementation of AGP, PCI and ISA buses in PC systems from 66 MHz to 100 MHz based on the 64 bit Socket-7 Super-scalar processors. The chipset is based on a north and a south bridge architecture; both bridges are acting as routers, routing data from one bus to another. The north bridge takes the heavy traffic and the south bridge routes in to a lot of different lighter routes. The VIA Apollo MVP3 is illustrated in Figure 2 within the chain dotted trapezium. The chipset comprises the system controller 28 identified as chip VT82C598 which acts as the north bridge, and a PCI to ISA bridge 30, implemented as chip VT82C586B, which acts as the south bridge. The system controller 28 provides superior performance between the CPU 10, optional synchronous cache (second level cache 14), DRAM 26, AGP bus 20 and the PCI bus 18 with pipelined, burst and concurrent operation. The controller 28 communicates with the DRAM over the memory bus 23 and supports standard fast pase mode (FPM), Extended Data Output (EDO), SDRAM and DDR SDRAM. The system controller also complies with the Accelerated Graphics Port Specification 1:0 and features support for 66/75/83/100 MHz CPU frequencies and 66 MHz AGP bus frequency. The PCI integrated peripheral controller forms a part of the chipset and supports Intel and non-Intel based processors to PCI bus bridge functionality to make a complete Microsoft PC97 - compliant PCI/ISA system. The peripheral controller provides ISA extension bus functionality and includes a number of intelligent peripheral controllers including a master mode IDE (Illustrated Drive Electronics) controller with dual channel DMA (direct memory access) engine and interlaced dual channel commands. High performance tranfers between devices connected to the PCI and IDE buses can be achieved through a dedicated FIFO coupled with scatter and gather master mode operation. Further intelligent peripheral controllers include a USB controller; a keyboard controller with PS2 mouse support; a real time clock with

256 byte extended CMOS; power management functionality which is compliant with ACPI (Advanced Configuration and Power Interface) and legacy APM (Advanced Power Management) requirements; distributed DMA capability for support of ISA legacy DMA over the PCI bus; PLUS and play control allowing steerability of all interrupts on the PCI bus to any interrupt channel; three additional screenable interrupt channels are provided to allow plug and play and reconfigurability of on-board peripherals for Windows 95 (TM) compliance; and external IOAPIC support for linked-compliant symmetrical multiprocessor systems.

Turning to Figure 3, the motherboard is configured to allow graphic accelerators to be connected to both the PCI bus and the AGP bus. The architecture shown in Figure 3 allows triple display screen configuration on a single board computer. Thus, in Figure 3, a PCI VGA controller 40 is attached to the PCI and, also to a TFT (thin film transistor) bus display. An AGP VGA controller 42 is connected to the AGP bus and has outputs which can support VGA, TFT or TV displays. The AGP VGA controller is also connected to an external memory 44. An MPEG II decoder 46 is attached to the PCI bus and coupled to the AGP VGA controller through the ATI multimedia channel (AMC) bus 48. This enables faster data throughput with minimum CPU intervention. It should be understood that each of the display controllers 40, 42 require addressing from only one of the PCI and AGP buses so doubling the driver capacity.

Turning now to Figure 4, the PCI and the AGP buses are both extended with twelve PCI VGA controllers 40 or graphics accelerators attached to the PCI bus, enabling twelve TFT displays to be driven and twelve AGP VGA controllers 42 attached to the AGP allowing twelve VGA monitors or a further twelve TFT displays to be driven. Thus, a total of twelve VGA or 24 TFT monitors can be driven simultaneously or independently of each other. To select the appropriate displays, the system BIOS will ID

select the PCI bus via the PCI integrated peripheral controller allowing efficient bus utilisation and at the same time select the AGP bus via the system controller giving the additional displays. Thus, the VGA controllers on the PCI bus are shown in Figure 4 as having device addresses AGP ID # 19-31. As in the embodiment of figure 3, the VGA controllers, the display controllers are each addressed from and connected to only one of the AGP and PCI buses doubling the number of display controllers that can be connected to the system.

It can be seen from Figure 4 that the AGP bus is driven by the system controller 28. A suitable graphical accelerator for use as the AGP VGA controller is the ATI 3D Rage LT Pro which has the advantages of providing high quality 2D and 3D performance, full motion DVD using motion compensation according to MPEG II standards, an integrated LVDS transmitter and tri-view architecture enabling simultaneous outputs to TV, CRT and LCD. Due to the tri-view feature, and in view of the configuration described with respect to Figure 3, it is possible to drive a monitor and a TFT display with one graphic accelerator on the AGP bus and one TFT display with one graphic accelerator on the PCI bus.

In summary, the embodiment of the invention described reconfigures the utilisation of the dedicated graphics bus, such as the AGP bus, and the general purpose bus, such as the PCI bus in a PC architecture. Rather than use the dedicated graphics bus solely for graphics data, the graphics bus is used also for display controllers. Thus, a separate display can be supported from both the graphics bus and the general purpose bus. These displays may be wholly independent of one another and display different types of data. By selection of a suitable graphic accelerator as one or both of the buses a number of displays of mixed type, for example TFT and CRT which is greater than the number of graphic accelerators. Each display controller is connected to only one of the

dedicated graphics bus, the AGP bus and the general purpose bus, the PCI bus, and requires addressing from only one bus so greatly increasing the number of display controllers that can be connected and, therefore, the number of displays that can be driven. It means that address locations on the two buses need only be resumed for display controllers that are connected to and driven by that bus.

By extending both the dedicated graphics bus and the general purpose bus, the number of graphic accelerators that can be attached to each bus is greatly increased. The use of a plurality of display controllers on each bus enable a much greater number of displays, of single or mixed type to be driven from a single PC motherboard having a single processor and a single system chipset. The number of display controllers which can be attached is limited by the size of the graphics and general purpose buses and also by the number of devices addresses which can be held in the system BIOS (basic input/output software). The BIOS software is stored in ROM 50 and so cannot be changed once set. At present it is possible to drive at least twelve display controllers of each bus. It is considered that twenty four display controllers may be possible for each bus as the standard BIOS commonly used assigns two device numbers to each display controller. A single device number is sufficient and by reassigning the remaining device number to a further display controller the number of controllers which can be accommodated is doubled.

Examples of TFT screens which can be connected include SVGA TFT, XGA TFT, UXGA TFT and Super TFT™. Each of these screens can provide touch screen capabilities. Other screens include Plasma and VGA monitors.

By using a VGA chipset which includes Low Voltage Differential Signalling (LVDS), a second display may be mounted 10-15m away from the base unit. This is advantgeous in many commercial and retail environments.

Thus, a multiple display with each screen running potentially independent application can be driven from the same PC processor using a single motherboard and chipset. This reduces considerably the cost per screen to a commercial organisation and has many potential applications, for example in the hospitality and retail industries. Suitable applications include EPOS (Electronic Point of Sale) touch screen terminals; promotional advertising; time of day promotions; children's games and loyalty type systems in a retail environment; interactive customer terminals; creation of lifestyle ambience via television, music etc; multimedia capabilities; kiosk terminals; and information distribution, for example in hotel environments directly to rooms at guests' request.

CLAIMS

1. A PC computer comprising a processor, a processor bus for transfer of data to and from the processor, a graphics bus, a general purpose bus for transfer of data to and from a plurality of input and output devices, a system chipset connected to the processor bus, graphics bus and general purpose bus comprising a plurality of controller devices for controlling the processor bus, the graphics bus and the general purpose bus, a first screen controller connected to the general purpose bus for controlling at least one display screen, and a second screen controller connected to the graphics bus for controlling at least one display screen; wherein the first and second screen controllers are each addressed from only one of the general purpose and graphic buses.

2. A PC computer according to claim 1, wherein the graphics bus is an accelerated graphics port (AGP) bus.

3. A PC computer according to claim 1 or 2, wherein the general purpose bus is a peripheral component interconnect (PCI) bus.

4. A PC computer according to claim 1, 2 or 3, wherein the system chipset comprises a system controller chip and a bridge chip arranged between the general purpose bus and a further input/output (I/O) bus, and wherein the graphics bus is connected to the system controller chip.

5. A PC computer according to claim 4, wherein the general purpose bus is connected between the system controller chip and the bridge chip.

6. A PC computer according to any preceding claim, wherein a video decoder is attached to the general purpose bus and to the screen controller on the graphics bus.

7. A PC computer according to claim 6, wherein the video decoder is an MPEG II decoder.

8. A PC computer according to claim 7, wherein the MPEG II decoder is connected to the screen controller on the graphics bus by a multimedia channel bus.

9. A PC computer according to any preceding claim, wherein at least one of the screen controllers connected to the graphics bus and the general purpose bus can output data simultaneously to two or more screens.

10. A PC controller according to claim 9, wherein said two or more screens comprise screens of different display types.

11. PC controller according to claim 10, wherein the display types include VGA monitors, TV screens and TFT screens.

12. A PC controller according to any preceding claim comprising a plurality of screen controllers attached to the graphics bus.

13. A PC computer according to any preceding claim, comprising a plurality of screen controllers connected to the general purpose bus.

14. A PC computer according to claim 13, wherein the general purpose bus has a number of expansion slots and the plurality of screen controllers is greater than the number of expansion slots.

15. A PC computer according to claim 12 and any of claims 6 to 8, wherein each of the plurality of screen controllers connected to the graphics bus is connected to the video decoder.

16. A PC computer according to claim 15, wherein the connection between each of the screen controllers and the video decoder is a multimedia channel bus.

17. A PC computer comprising a central processor unit (CPU) having a CPU bus associated therewith for transfer of data to and from the CPU, an accelerated graphics port (AGP) bus communicating with a graphics controller, a peripheral component interconnect (PCI) bus communicating with a plurality of peripheral components, a system chipset comprising a system controller communicating with the AGP bus, and a bridge communicating with the system controller and a plurality of further buses and devices, wherein the PCI bus communicates with the system controller and the bridge, at least one first screen controller communicating with the PCI bus, and at least one second screen controller communicating with the AGP bus, the first and second screen controllers each being addressed by one only of the PCI and AGP buses.

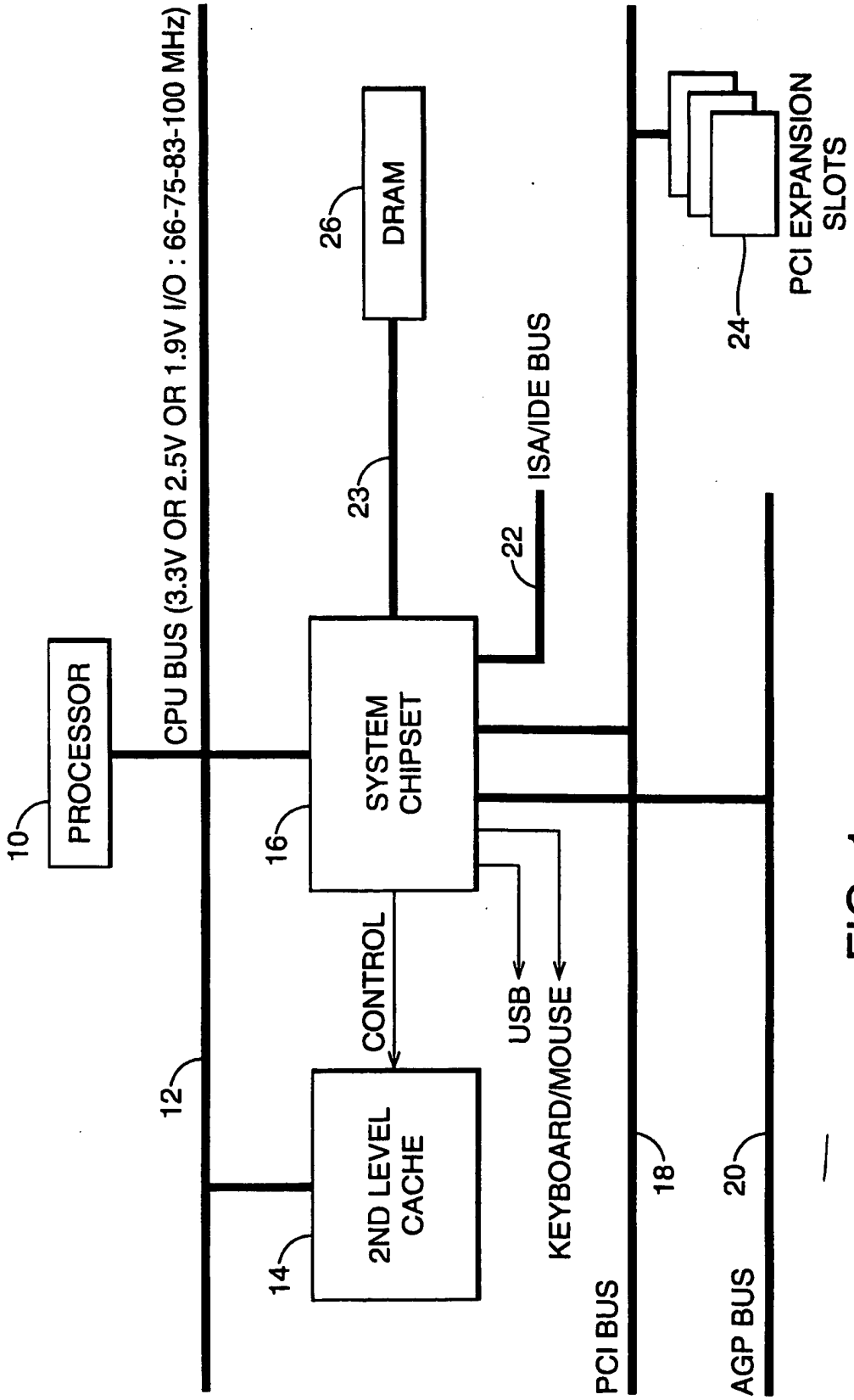

FIG. 1 STANDARD PC CONFIGURATION

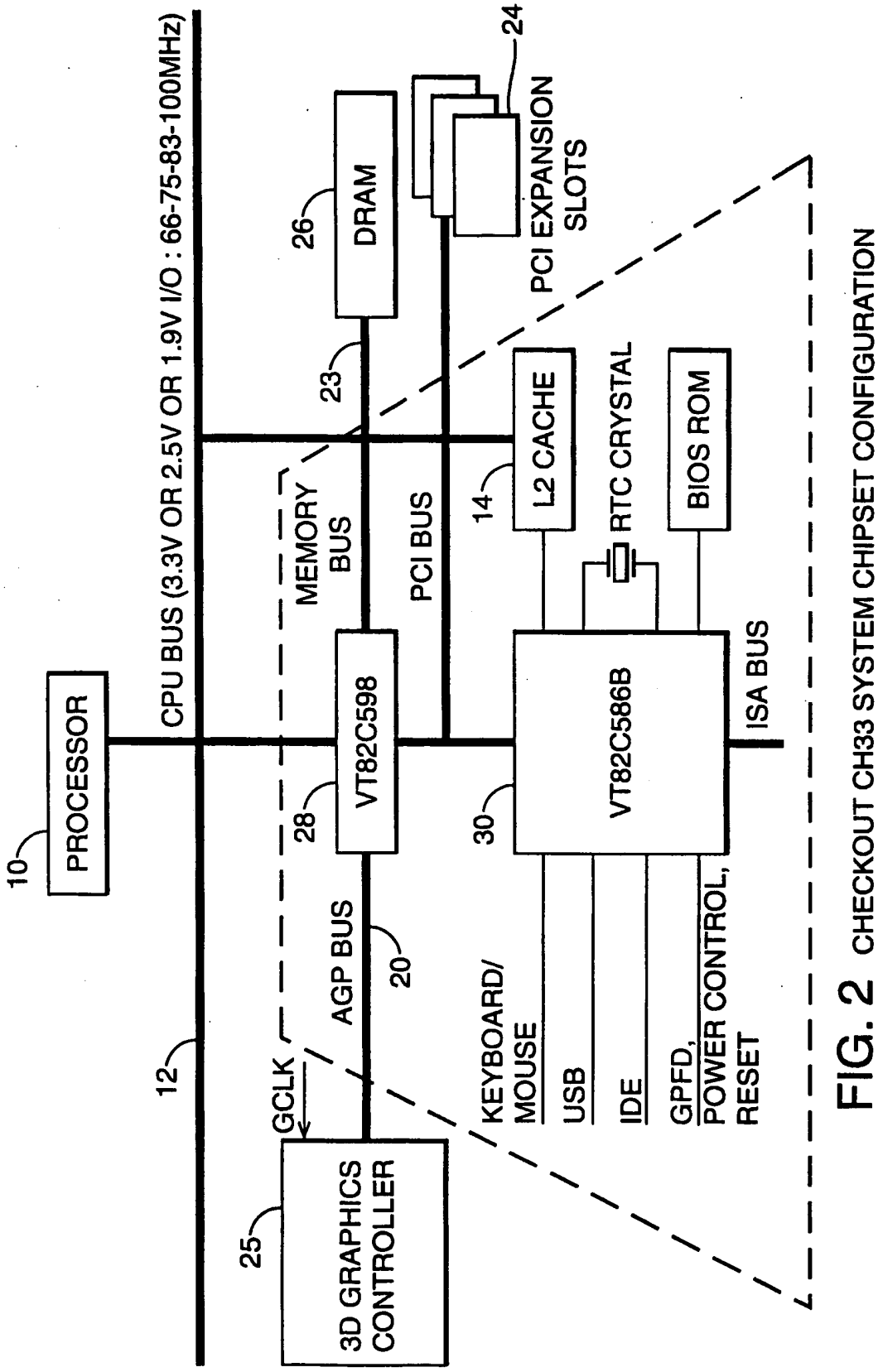

FIG. 2 CHECKOUT CH33 SYSTEM CHIPSET CONFIGURATION

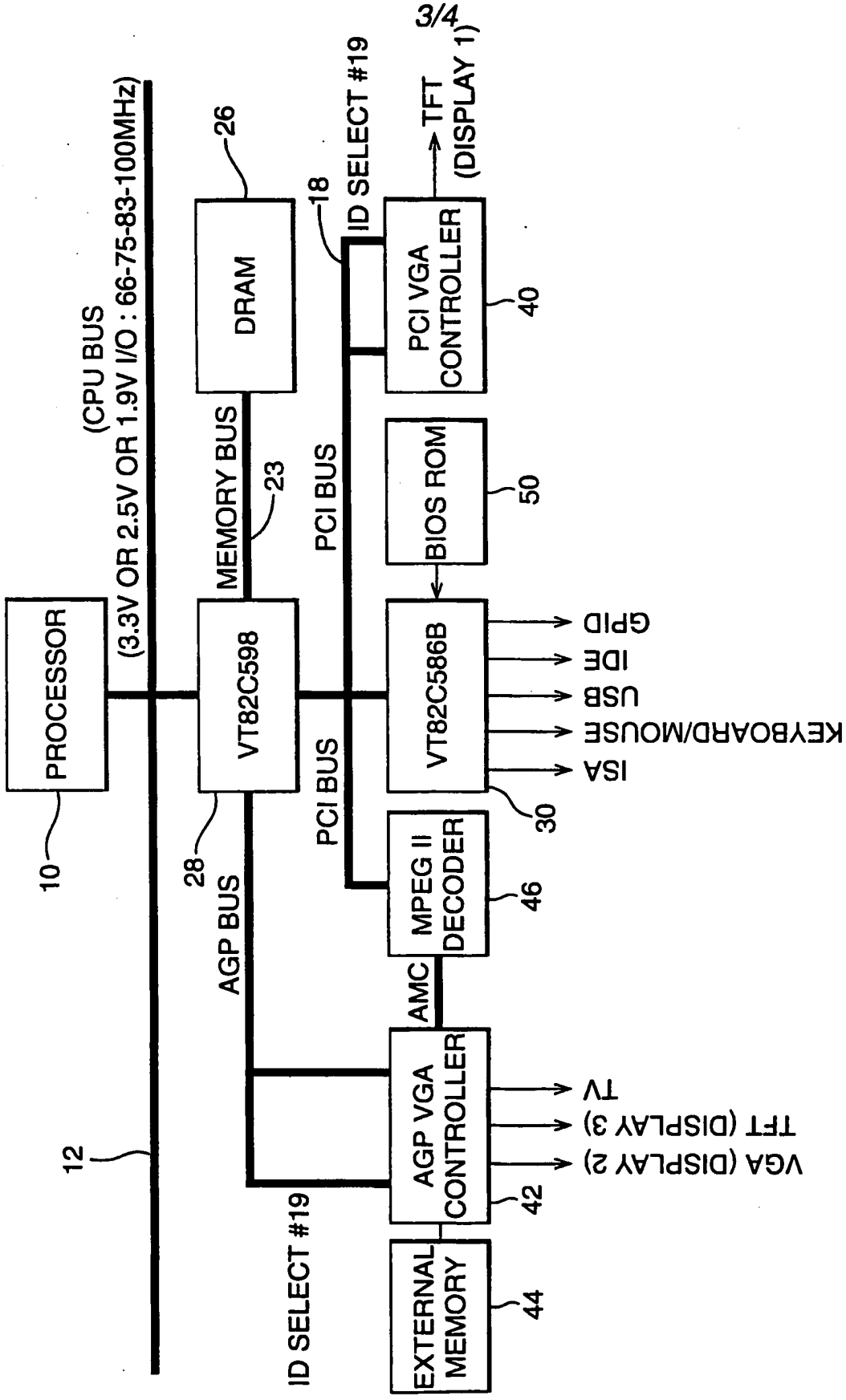

FIG. 3 CHECKOUT CH33 TRIPLE SCREEN CONFIGURATION

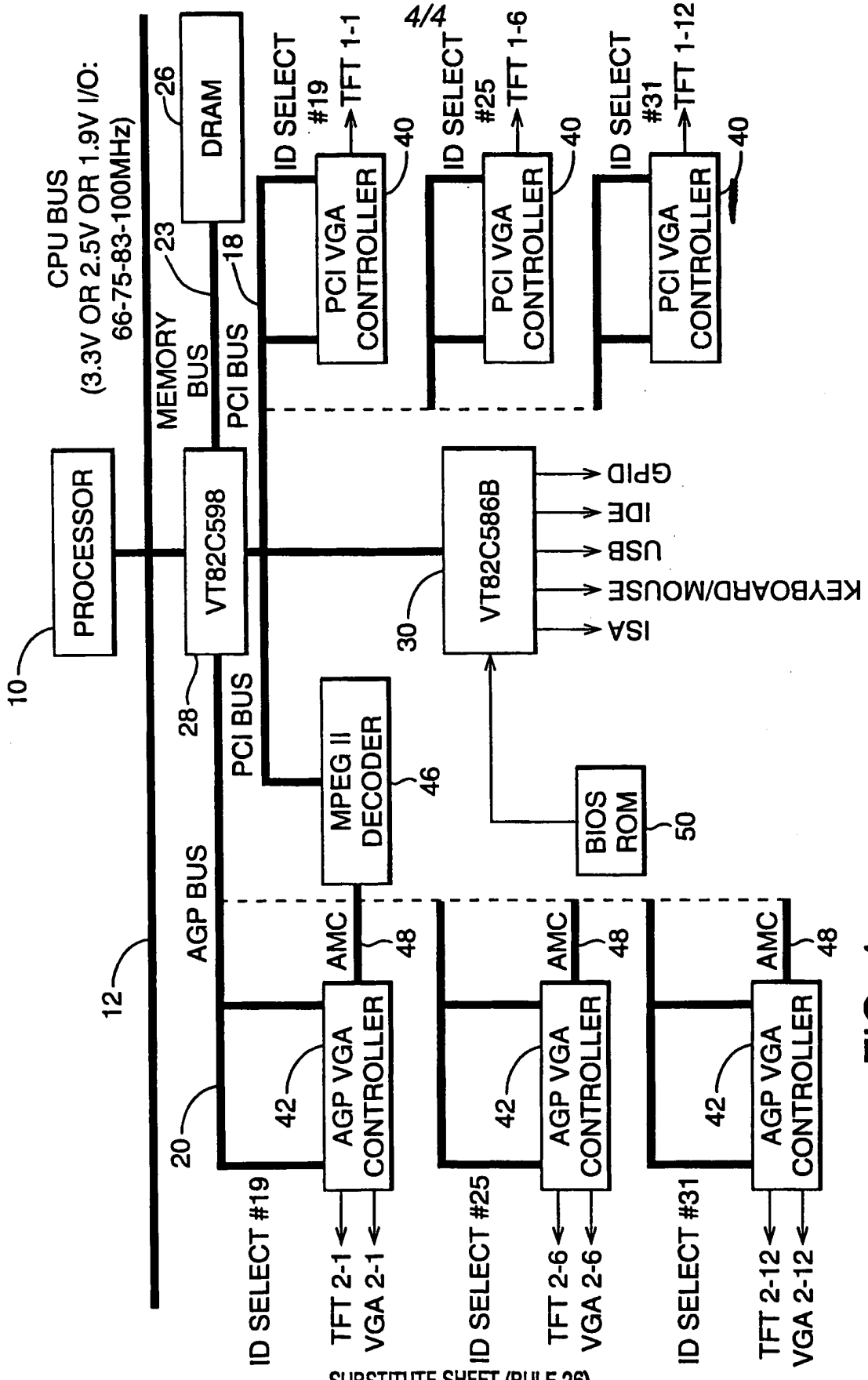

FIG. 4 CHECKOUT CH33 EXTENDED MULTISCREEN CONFIGURATION

INTERNATIONAL SEARCH REPORT

Interr ·al Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F3/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"Accelerated Graphics Port Interface Specification Revision 2.0" 'Online! 4 May 1998 (1998-05-04) , INTEL CORPORATION XP002123870 Retrieved from the Internet: <URL: http://www.intel.com/technology/agp/agp_index.htm> 'retrieved on 1999-11-17!	1-5,17
Y	paragraphs '01.2!,'6.1.2!,'6.1.3.4!,'6.1.4!,'06.2!,'06.3!	9-13
Y	US 5 488 385 A (SINGHAL DAVE M ET AL) 30 January 1996 (1996-01-30) column 4, line 9 -column 5, line 61	9-13
A	column 1, line 19 -column 2, line 24	14

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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PCT/GB 99/02854

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 814 401 A (TEXAS INSTRUMENTS INC) 29 December 1997 (1997-12-29) column 3, line 52 -column 5, line 16; figure 2	6

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interr nal Application No
PCT/GB 99/02854

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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EP 0814401 A	29-12-1997	US 5841994 A	24-11-1998
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